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ELECTRONIC PROCESSES IN InP AND RELATED COMPOUNDS

LEVEL II

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K. V. Vaidyanathan, C. L. Anderson, D. E. Holmes, and G. S. Kamath

Hughes Research Laboratories
3011 Malibu Canyon Road
Malibu, CA 90265

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The report describes liquid phase epitaxial growth of indium phosphide. The electrical and luminescence properties of such layers are discussed. Ion implantation doping and encapsulant-free annealing studies are discussed.

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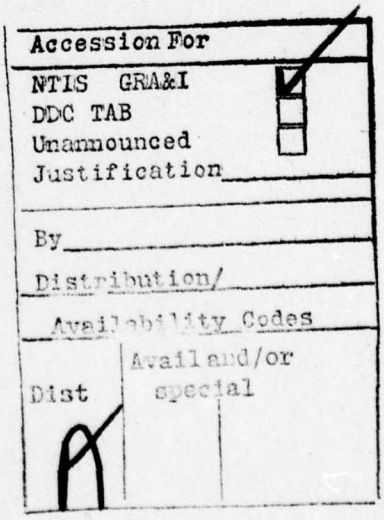

SECTION 1

INTRODUCTION AND SUMMARY

This report discusses the technical progress achieved during a four-month study of electronic processes in InP and related compounds. Two areas were emphasized during this phase of the contract:

- Optical and electrical characterization of bulk and epi InP
- Investigation of doping of InP to form p-n junctions.

During the initial phase of this program, we evaluated the parameters that influence the liquid phase epitaxial (LPE) growth of InP layers. Using internal funds, we have also made preliminary ion implantation doping studies and established that our melt controlled ambient technique (MCAT) can be successfully used to anneal the implant damage and to electrically activate the implanted impurities. Some implanted samples have also been annealed with a pulsed electron beam (E beam). Our initial results indicate that the electron fluence used in these studies was too high, thus resulting in considerable loss of phosphorus. More detailed studies of E-beam annealing of ion-implanted InP are presently underway.

During the second phase of the program, we propose to investigate the ion implantation doping of InP and InGaAsP materials and to perform ionization rate measurements as soon as suitable device structures become available.

SECTION 2

EPITAXIAL GROWTH OF InP

High purity InP and quaternary $In_{(1-x)}Ga_xAs_yP_{(1-y)}$ layers can be grown by LPE.[1-4] Two variations of the LPE technique are commonly used: the slide-bar technique using small solutions (the limited melt technique) and the dipping technique using larger solutions (the infinite solution technique). The slide-bar technique has the disadvantage that severe melt depletion effects occur after a few layers have been grown. This reduces the number of layers with reproducible properties that can be grown from a single melt. This especially may be a problem in the growth of quaternary layers. In contrast, the infinite solution technique, in principle, allows several hundred layers with reproducible properties to be grown from the same melt.

Hughes Research Laboratories (HRL) has developed a unique variation of the infinite solution growth technique. This variation, illustrated in Figure 1, consists basically of an all-quartz growth tube connected by a high-vacuum valve to a stainless-steel entry chamber. A saturated solution of the appropriate elements serves as the growth matrix. Once a specific solution has been prepared, it is kept in a palladium-purified hydrogen ambient. It can thus be maintained at or near the growth temperature in a controlled environment for months. During a long series of runs, all epitaxial growth operations (such as introducing substrates or adding dopants) are performed by passing these materials through an entry chamber, which can be independently evacuated and flushed with hydrogen before opening to the growth tube. It is thus possible to maintain a high-purity solution for a period of months. The growth ambient can also be conveniently changed while all other variables are kept under control. This capability is extremely advantageous in growing high-purity InP layers and is discussed in detail later in this section.

Table 1 shows the results obtained from several typical epitaxial layers. The high mobilities observed are indicative of the purity of the epitaxial layers. Figure 2 shows the variation in doping

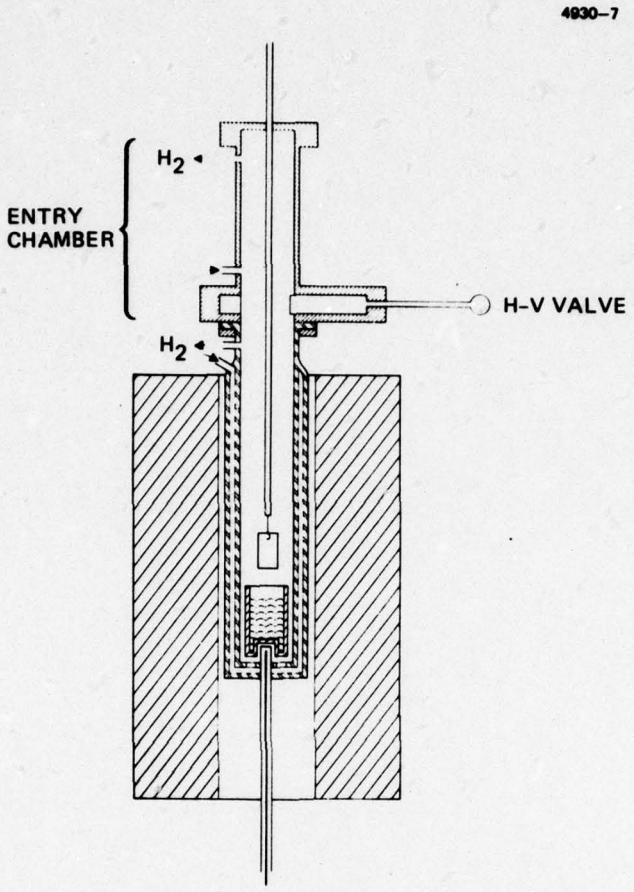

Figure 1. Liquid phase epitaxial growth system.

concentration as a function of distance into the epitaxial layer at various points over a large Sn-doped wafer (1 x 1-1/4 in., shown in inset). This represents the doping homogeneity that can be obtained in layers grown by the infinite solution system.

The performance of optoelectronic devices depends critically on the ability to grow uniform, thin, homogeneous and dislocation-free epitaxial layers. Also, in devices involving heterojunctions, it is necessary to reduce defects at the interface. To satisfy all these requirements, the surfaces must see a uniform growth ambient (a chemically homogeneous growth matrix and uniform temperature over the growth surface), and the layers must be grown slowly enough to permit near-equilibrium conditions to be established at the growth interface.

Table 1. Characteristics of Several Typical Epitaxial Layers

Material	Layer No.	Layer Thickness, μm	Type	Carrier Concentration, cm^{-3}	Hall Mobility, $cm^2\ V^{-1}sec^{-1}$
GaAs[a]	370	10	p (undoped)	2×10^{14}	420
GaAs[a]	126	7	n(Sn)	7×10^{15}	5900
GaAs[a]	211	1	n(Sn)	2×10^{16}	4800
GaAs[b]			n (undoped)	2×10^{15}	6620
$Ga_{0.96}Al_{0.04}As$	20	56	p (undoped)	9×10^{13}	319
$Ga_{0.6}Al_{0.4}As$	47	13	n(Sn)	8×10^{14}	1724
$Ga_{0.3}Al_{0.7}As$	80	5	p(Ge)	1.3×10^{18}	138
$Ga_{0.94}In_{0.06}As$	295	45	n (undoped)	5×10^{15}	5400

[a]Layer grown with commercially available bulk GaAs as solute.

[b]Layer grown with GaAs leached at ∿450°C for several days prior to dissolution.

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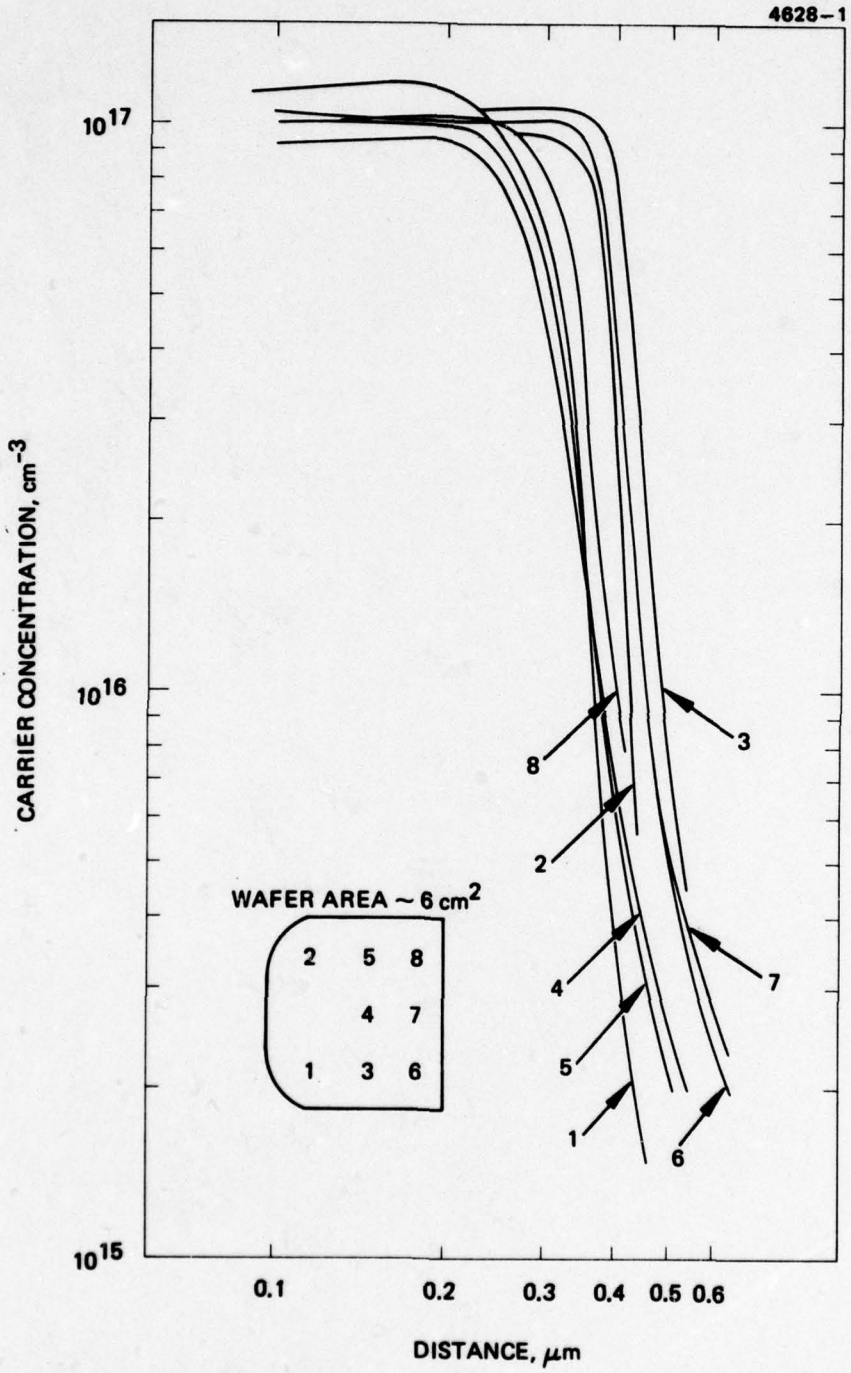

Figure 2. Epilayer doping concentration versus distance profiles at various points on the wafer shown in the inset.

We have developed a graphite sample holder assembly to house the substrate (Figure 3) that allows us to operate under such conditions. The substrate is introduced into the melt within the sample holder, and the whole assembly rotates in the melt until temperature equilibrium is fully established. This rotation further helps to ensure good mixing and homogeneity in the melt. By raising the graphite cover, the sample is exposed to the melt. Growth is stopped by (1) closing the cover; (2) raising the sample holder out of the solution; and (3) reopening the cover, at which point the solution trapped in the sample holder falls out. Note that at no time in the growth procedure does the surface of the sample pass through the meniscus on the solution. Furthermore, the cover of the sample holder does not wipe the melt from the sample. Using this technique, we have grown thin epitaxial layers with excellent surface morphology and reproducible electrical properties.

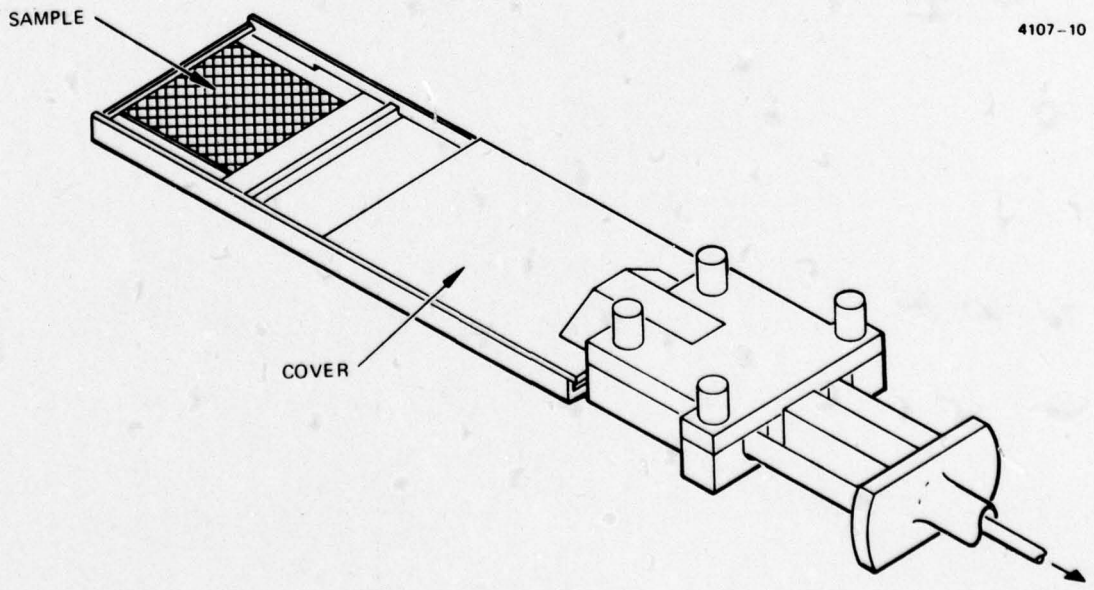

Figure 3. Graphite slide-bar assembly.

Using the infinite solution growth technique, we have successfully grown high-purity InP epitaxial layers with carrier concentrations of $\sim 3 \times 10^{15}$ cm^{-3} and room-temperature mobilities of ~ 4000 cm^2 V^{-1} sec^{-1}. The surface morphology of these layers grown at 630°C is smooth. Extensive Hall-effect measurements have been made as a function of temperature. The data can be analyzed to yield values of donor concentration (N_D), acceptor concentration (N_A), and degree of compensation. Mobilities as high as 41,000 cm^2 V^{-1} sec^{-1} at 77°K have been measured. The compensation ratio as determined from these measurements lies in the range of 0.5 to 0.6. This agrees very well with theoretical calculations.[5]

Low-temperature photoluminescence (PL) is very sensitive to the total impurity concentration in the sample. It is a relatively simple qualitative tool. The photoluminescence spectra obtained from two of our typical epitaxial layers are shown in Figure 4. Spectrum (a) was obtained from a layer that had a net impurity concentration of 8.5×10^{16} cm^{-3}. The spectrum is dominated by emission bands at ~ 1.419 eV and ~ 1.385 eV. The band at 1.419 eV consists of a doublet and is related to the band edge emission. As expected, the width of this emission band is relatively large. The 1.385 eV emission probably involves donors and acceptors. In contrast, spectrum (b) exhibits a much narrower band edge emission. The two peaks are also clearly defined, indicating that the material is of higher purity. The electrical measurements show that this sample has a net impurity concentration of 3.6×10^{15} cm^{-3}. An interesting feature is the absence of the lower energy emission at 1.385 eV.

The combination of electrical and optical measurements shows that high-purity epitaxial layers can be reproducibly grown using the infinite solution growth technique. All the growth studies were performed using internal funds.

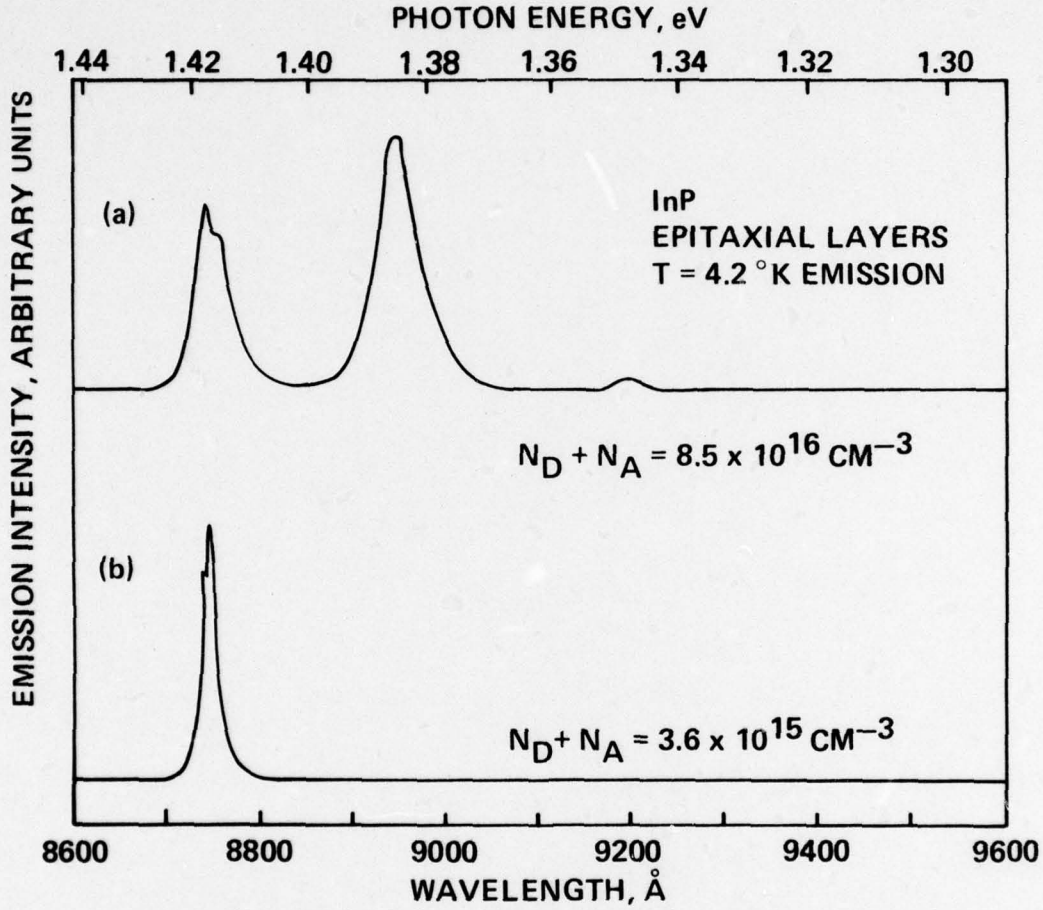

Figure 4. Photoluminescence spectra of InP.

SECTION 3

ION IMPLANTATION STUDIES

Ion implantation is a versatile method of introducing impurities in semiconductors. The technique allows controlled doping, both in terms of concentration and of the depth of the doped layer. However, the process introduces considerable lattice disorder, which must be annealed out to activate the impurities electrically. For most compound semiconductors, the temperature required for such an anneal is higher than its dissociation temperature. For instance, the required anneal temperature is between 800 and 900°C for GaAs and in excess of 550°C for InP. It is necessary to prevent the loss of the volatile group V component during annealing. For GaAs, this is usually achieved by encapsulating the sample with either SiO_2 or Si_3N_4 layers before they are annealed.

We have successfully annealed InP at 650°C with SiO_2 encapsulation, while other workers have used phosphosilicate glass (PSG) as an encapsulant.[6,7] Using internal funds, we are presently establishing a system capable of depositing PSG layers for encapsulating InP and $In_{1-x}Ga_xAs_yP_{1-y}$.

The samples can also be annealed in a controlled ambient that prevents decomposition of the sample. We have developed a novel encapsulant-free annealing technique — called the melt controlled ambient technique (MCAT) — for annealing III-V compound semiconductors. The technique uses the infinite solution growth system described in Section 2. The saturated solution (or the melt) provides the required controlled ambient for annealing.

The experimental procedure consists of placing the samples to be annealed in a suitably conditioned, specially designed wafer holder and then immersing the holder in the solution at the required anneal temperature. Although the samples are not in physical contact with the solution, they are in vapor contact. The results obtained from MCAT, Se-implanted GaAs samples are shown in Figure 5.[8] These studies, performed under an AFOSR contract, show that activation superior to any reported results can be achieved in GaAs. We have performed annealing studies (some under

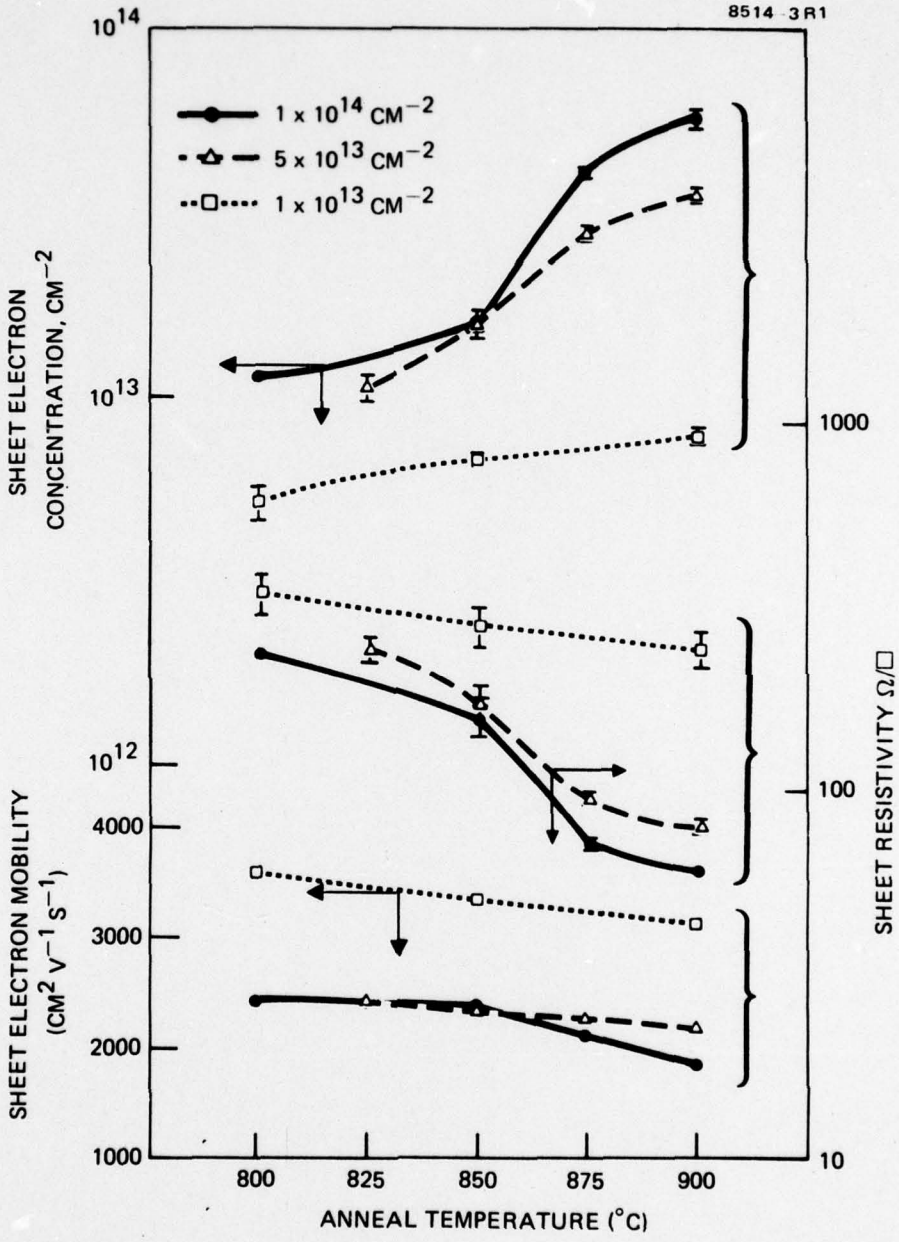

Figure 5. Electrical properties of 250°C Se-implanted, MCAT-annealed GaAs.

this contract) of ion-implanted InP samples using the MCAT approach. The initial results (Table 3) have been highly encouraging. It is remarkable that considerable electrical activation has been observed even at an anneal temperature as low as 580°C. For comparison, the results obtained from samples encapsulated with SiO_2 and annealed at 650°C are also shown in Table 2. These results show that MCAT annealing can be extended to InP and possibly to the quaternary $In_{1-x}Ga_xAs_yP_{1-y}$.

An intense pulsed E beam can be used to anneal ion-implantation damage in Si and GaAs. We have performed E-beam annealing studies of ion-implanted GaAs and InP. The E beams used in these studies had a mean energy of 30 keV and were obtained by discharging cylindrical capacitors. These studies were performed at the Spire Corporation, Bedford, Massachusetts. The results obtained from GaAs samples are shown in Table 3.[9] The E-beam fluence is roughly proportional to the charging voltage shown in the table. These results, especially for the 5×10^{14} cm^{-2} implanted samples, are far superior to any published data. The data from InP samples is, however, not so spectacular. For all the E-beam fluences used in the preliminary studies, considerable loss of phosphorus occurred, resulting in the formation of indium-rich surfaces. The surface morphology, however, was very good. More detailed investigations of E-beam annealing are necessary.

Table 2. Annealing of Ion-Implanted InP

Ion	Thermal Anneal (650°C) Silox Oxide			MCAT Anneal (570°C)		
	Sheet Resistivity, Ω/□	Mobility, $cm^2\ V^{-1}\ sec^{-1}$	Apparent Electrical Activation, %	Sheet Resistivity, Ω/□	Mobility, $cm^2\ V^{-1}\ sec^{-1}$	Apparent Electrical Activation, %
S	316 ± 24	921 ± 32	21.6	194	1239	26
Si	435 ± 6	1580 ± 50	9.1 ± 0.5	620 ± 10	1680 ± 10	6 ± 0.2
Sn	1680 ± 110	160 ± 50	25 ± 6	1230 ± 500	480 ± 10	13 ± 5

S: 120 keV, $10^{14}\ cm^{-2}$

Si: 120 keV, $10^{14}\ cm^{-2}$

Sn: 240 keV, $10^{14}\ cm^{-2}$

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Table 3. Electrical Properties of E-beam-Annealed GaAs

Implanted Impurity	Dose, cm^{-2}	Charging Voltage, kV	Sheet Resistivity, Ω/□	Hall Mobility, $cm^2V^{-1}sec^{-1}$	Sheet Electron Concentration, cm^{-2}
Se	1×10^{14}	145	514	609	1.9×10^{13}
Se + Ga + As	1×10^{14} 5×10^{14} 5×10^{14}	155	481	887	1.46×10^{13}
Se	5×10^{14}	160	68	804	1.15×10^{14}
Se + Ga + As	5×10^{14} 5×10^{14} 5×10^{14}	155	67	647	1.45×10^{14}
Si	1×10^{14}	160	2612	575	4.16×10^{12}
Si + Ga + As	1×10^{14} 5×10^{14} 5×10^{14}	155	320	980	2.0×10^{13}
Si	5×10^{14}	175	89	940	7.5×10^{13}
Ga + As + Si	5×10^{14} 5×10^{14} 5×10^{14}	160	68	780	1.2×10^{14}

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SECTION 4

DEVICE PROCESSING STUDIES

In the fabrication of avalanche photodiodes, it is necessary to develop a suitable technology for forming either mesa-etched or planar-isolated p-n junctions. We have performed studies aimed at developing localized implantation doping and mesa etching capabilities in InP. The results are summarized in this section.

To form planar isolated p-n junctions, it is necessary to develop a masking scheme that will prevent ions from penetrating into unwanted regions. A photoresist mask, although simple to use, polymerizes when exposed to an intense ion beam and often results in unwanted carbon contamination. We have developed a unique implant mask consisting of plasma-deposited silicon oxynitride and germanium films. These layers are deposited at relatively low temperatures. Plasma etching can be used to define the localized regions. Figure 6 shows an SEM photograph of a sample ready for implant with such a mask.

To develop a suitable etch for forming mesas, we have investigated several wet chemical etches. In each case, the etch rate decreased considerably after the first few minutes of etching. Auger electron spectroscopy (AES) analysis of the etched surface reveals the presence of a stable indium oxide layer (Figure 7) at the surface. We believe that this layer retards further chemical reactions. We are presently investigating the possibility of combining dry plasma etching along with wet chemical etching to alleviate this problem.

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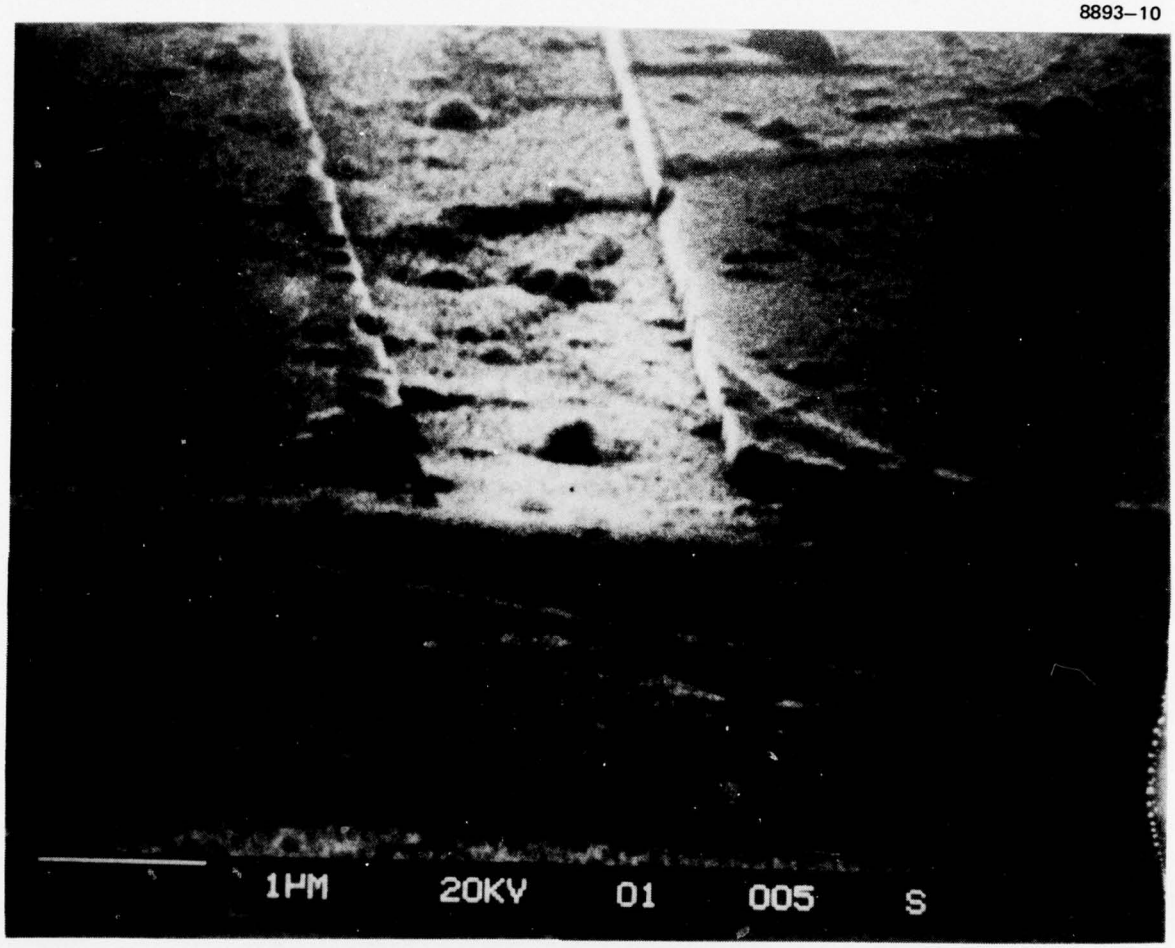

Figure 6. SEM photograph of a 1.5-μm-wide stripe formed by plasma etching of Ge deposited over silicon oxynitride on GaAs. The silicon oxynitride-germanium layer will be used as an implant mask.

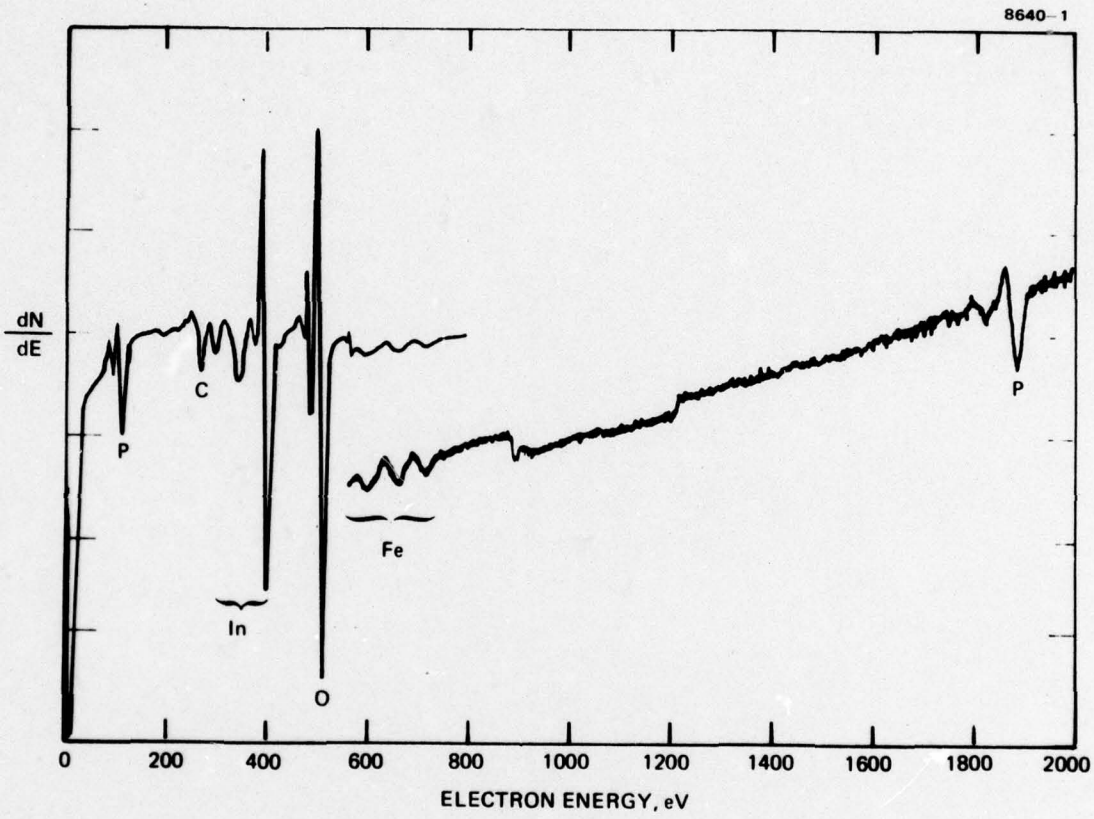

Figure 7. Auger electron spectrum obtained from a chemically etched InP sample showing the formation of oxide of indium on the surface.

SECTION 5

IONIZATION COEFFICIENT MEASUREMENTS

In general, avalanche photodiodes are subject to more stringent requirements which relate to the interaction of hole and electron multiplication in the high-field region of the diode and to the prevention of local regions of premature avalanche breakdown. It is essential that the avalanche photodiode design provide for the efficient collection of light and the rapid transport of the photogenerated carriers to the high-field region. A uniform region of high field in which avalanche multiplication takes place can be obtained using Schottky barriers or reverse-biased p-n junctions. It is essential that such junctions be fabricated in crystals that are free from local regions of premature breakdown both in the bulk of the semiconductor (microplasmas) and at the surface. Surface breakdown can be prevented by using concentric Schottky-barrier guard rings or by deep n diffusions under the periphery of an n^+-p avalanche photodiode[10] to increase the breakdown voltage. Surface electric fields can also be reduced by shaping the diode to form a mesa.[11] More recently, ion implantation has been used to create high-resistivity regions in the semiconductor to prevent edge breakdown.[12]

Avalanche photodiode design depends critically on the relative magnitudes of the electron and hole ionization coefficients ($\alpha(E)$ and $\beta(E)$, respectively). For $\beta(E)/\alpha(E)$ ratios significantly larger or smaller than one, the multiplication is a more slowly varying function of reverse bias voltage, which thus places less stringent demands on bias stability.[13] Photo-induced carriers of the type with the highest ionization coefficient should be introduced into the high-field region to maximize the low-frequency avalanche gain. The product of avalanche gain and bandwidth is also maximized by using a semiconductor with a value of $\beta(E)/\alpha(E)$ much larger or smaller than one.[14] Since excess noise introduced by the multiplication process is minimized under these conditions,[15] it is important to determine the ionization coefficients for a given semiconductor before deciding on photodiode design details.

Ionization coefficients have been measured on various semiconductors over the years and are still being refined. Chynoweth[16] has pointed out some of the conditions that should be met in the ideal experiment:

- Pure electron or hole injection should be used in the same junction rather than in complementary junctions.
- The profile and magnitude of the field in the junction should be accurately known.
- The external quantum efficiency without avalanche gain should be accurately determined and not vary with low diode bias voltages.
- The structure should be free from microplasmas over the bias range used in the measurements.

We are in the process of assembling an experimental set up (shown schematically in Figure 8) to measure ionization coefficients in InP and $In_{1-x}Ga_xAs_yP_{1-y}$. It consists of two stable He-Ne lasers capable of operating at 0.6328 μm and 1.152 μm. The experiments will be controlled by a HP 9825A calculator and will be available for ionization coefficient measurements by September 1979.

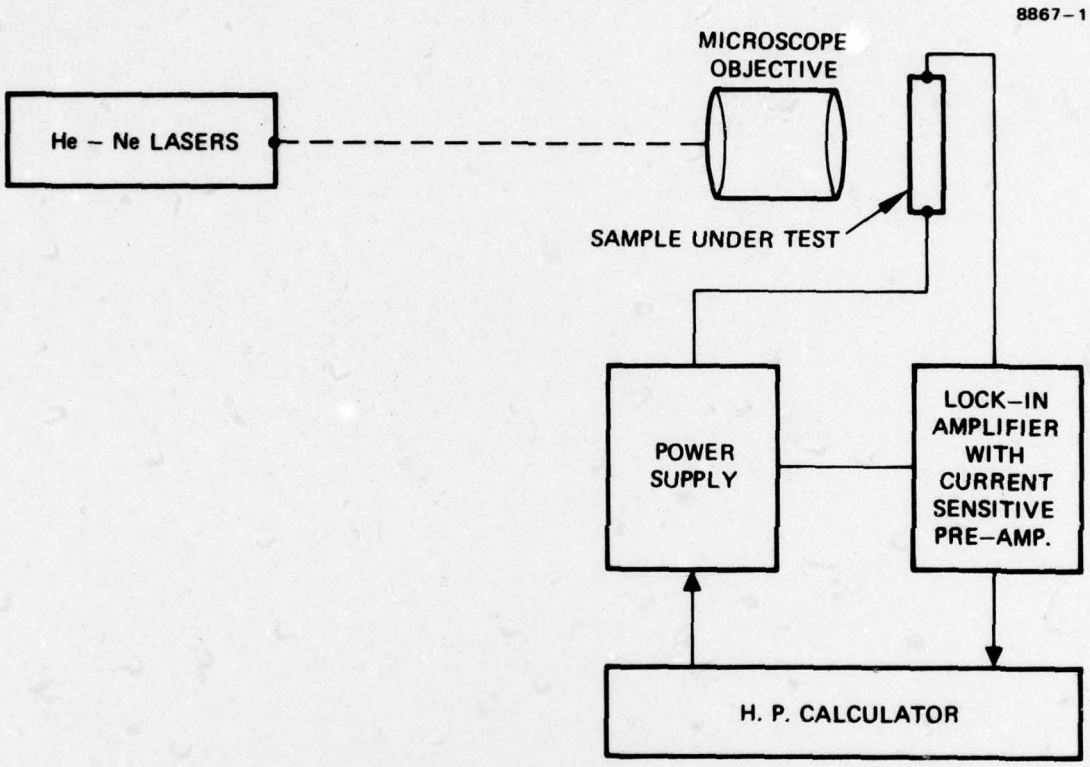

Figure 8. Experimental setup for ionization coefficient measurements.

SECTION 6

SUMMARY

The results discussed in the previous sections of this report are summarized below.

In the area of epitaxial growth, we have demonstrated that high-purity epitaxial layers with carrier concentrations of $\sim 3 \times 10^{15}$ cm^{-3} and room-temperature mobilities of $\sim 5{,}000$ $cm^2V^{-1}sec^{-1}$ can be reproducibly grown by the infinite solution growth technique. To achieve this growth, it is necessary to have small ($\sim$1 ppm) amounts of water vapor in the gas stream. We have developed a model that consistently explains our epitaxial growth results. Photoluminescence spectra obtained from layers grown with or without water vapor present in the growth ambient exhibit significant differences. These photoluminescence data correlate very well with the electrical properties of these layers.

Ion implantation doping studies demonstrate that the melt controlled ambient technique (MCAT) can be extended to the annealing of implantation damage in InP and may offer significant advantages over annealing techniques employing deposited dielectrics.

Experiments aimed at developing localized implantation and mesa etching techniques for device fabrication in InP are discussed. A calculator controlled experimental setup for determining ionization coefficient measurements is being established.

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